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RDL Copper Plating Process for Panel Level Packaging Application

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ABSTRACT

Advanced packaging suppliers are having two primary challenges during IC substrate fabrication, meeting the requirements on copper plating performance and reducing the cost from manufacturing process. The requirements on plating performance include high resolution and strict height uniformity within a die (WID) and within a panel (WIP), consistent deposit grain structure, and robust physical properties to meet reliability requirements. The plated features include fine lines, trenches, and vias, whose top shape and coplanarity are critical to the product quality. A non-planar surface could result in signal transmission loss and introduce weak points in the connections. Therefore, copper plating solutions providing uniform, planar structures, without any special post treatment are highly desirable features from RDL plating processes. The copper plating solution can also reduce cost by plating two or three types of features in a single electrolyte, this flexibility allows fabricators to save on space and equipment

In this paper, an electroplating package, Systek UVF 200, is introduced to plate RDL under different current densities in vertical continuous platers (VCP) and a high-speed panel plater. The plating uniformity was evaluated on a panel level in a high-speed plater, AMSPT NEXX P500.

The Systek UVF 200 package offered excellent coplanarity within a pattern unit or die for RDL plating. The variation in the plated height (or thickness) between fine lines (as low as 9 µm in width) and pads, was below 2.0 µm when using a current density below 5.0 ASD to obtain the plated copper thickness around 12 µm. For 14 µm wide lines, the plated copper thickness variation can be below 1.2 µm. The variation of plated thickness across 510 mm x 515 mm panels was below 5%. The tops of the fine lines have defined, slightly domed shapes, these types of profiles have excellent conductivity.

Physical properties of the plated copper deposit are essential for the reliability of the finished product. A few key physical properties are tensile strength, elongation %, and internal stress. These properties show the tolerance of the deposit to withstand thermal stress and warpage. The additives (wetter, brightener, and leveler) strongly influence the physical properties of the deposit. Copper deposited with the Systek UVF 200 package has tensile strength above 40,000 psi, elongation % above 18%, and internal stress below 1.0 Kg/mm^2. The physical properties of the deposited copper did not change under different current density, showing that the package has stable performance.

INTRODUCTION

RDLs (Redistribution Layers) are typically metal interconnection schemes or metal traces that route the electrical signals from one part of the package to another. The formation of the redistribution layer is focused on semi-additive processing (SAP), which utilizes dielectric isolation layers, seeding layers by physical vapor deposition (PVD) or electroless copper, high resolution photomask formation, electrolytic copper plating, a final stripping of the photo resist, and differential etching of seed layer. In the case of a high-density fan-out wafer-level packaging (FOWLP), multiple layers of RDL are required to support the necessary routing. The metal traces together with dielectric isolation layers generate multi-layer RDLs. The scaling from wafer-level to panel-level is expected to be the next evolution of fan-out (FO) packaging. However, there is still a technical gap between wafer technologies and panel level processing. One major technological challenge to close this gap is to lower the structure size of lines and spaces (L/S) significantly. While L/S is going smaller, panel size is going up to 510 mm x 515 mm or possibly larger. On the performance front, a key problem to be solved is to obtain both high resolution and height uniformity within the RDL fine line during copper plating process. This is especially true when the design includes ground planes, fine lines, and microvias, all to be plated simultaneously with what is called 2-in-1 RDL plating. Plating uniformity, trace and via top shapes and coplanarity are critical to signal transmission. A non-planar surface could result in signal transmission loss and induce stress points to the connection. Therefore, copper plating solutions providing uniform, planar profile without any special post treatment are highly desirable features of fine line RDL plating processes. It requires a specially designed copper plating chemistry as well as a plating chamber design to achieving high-quality uniformity at the highest plating rates. In this paper, the acid copper plating processes are explored for the plating capability on 2-in-1 RDL technologies. The electrolyte, Systek UVF 200, was evaluated on plating uniformity and coplanarity of both fine line RDL and microvias on panel level plating (PLP) with a high-speed plater, AMSPT NEXX P500.

Systek UVF 200 on 2-In-1 RDL Plating and Via Filling

SAP has been used for making fine lines on organic substrates for decades, the process begins with electroless copper plating to form an ultra-thin conductive seed layer, followed by photolithography to pattern a photo resist on the surface. Copper electrolytic plating is then used to form metallization structures between the photo resist patterns. This is then followed by removal of photo resist and micro-etching (differential etch) of the copper seed layer to complete the patterning. SAP processes have advanced enough to allow wiring dimensions down to 6-9 µm, but due to the small amount of side etching that occurs to the plated copper during the seed layer removal process, there has been a challenge in reducing line width scales further. The finest line in this evaluation was 9 µm on the panels that was 510mm x 515 mm in size, plating thickness varies depending on the panel design and OEM requirements.

The electrolyte, branded as Systek UVF 200, was used as shown below in Table 1. The plating evaluation was processed in a vertical continuous plater (VCP) to obtain the electrolyte plating performance within a die (WID) or withing a unit (WIU), then AMSPT NEXX P500 plater was used to evaluate the uniformity within panel (WIP). The test panels have a photo imaged dry film patterns on electroless copper seed layer, dryfilm thickness at 25 µm. Each test panel that was plated in a VCP went through a pre-clean cycle of 1 min acid cleaner, 1 min rinse, 1 min 10% sulfuric acid before the plating in the acid copper containing the Systek UVF 200 electrolyte as described below.

SYSTEK UVF 200	Chemistry	Concentration
VMS	$CuSO_4$	200-240 g/L
	H_2SO_4	40-120 g/L
	Cl^-	50 ppm
Additives	Wetter	10 ml/L
	Brightener	5 ml/L
	Leveler	2 ml/L
Parameter	CD	1.0-6.0 ASD
	Temperature	25 & 35 ºC

Table 1. Systek UVF 200 electrolyte and plating parameters

Typical acid copper electrolytes contain copper sulfate, sulfuric acid, chloride ions, and organic additives. These additives play a crucial role in controlling the deposit distribution as well as the copper deposit physical properties. To meet specific objectives of a plating process these additives should be monitored and controlled properly. The additives work in combination when they are controlled within a given range to improve plating uniformity. Namely these additives are Wetter (or Suppressor), Brightener (or Accelerator), and Leveler. The wetter works in the presence of chloride ion to adsorb on to the cathode and increase the effective thickness of the diffusion layer. As a consequence, the plating current increases and the deposit becomes more uniform and a densely packed copper deposit can be obtained without burning. This modified diffusion layer improves the distribution of the deposit especially in fine line plating. Brightener is also called an anti-suppressor or accelerator, and as the name implies it reduces the suppression. Most importantly it also acts as a grain refiner to deposit copper with a fine grain structure in random orientation. Therefore, brightener has the most influence on final structure and physical properties of the deposit such as tensile strength and elongation. The leveler is a mild suppressor that adsorbs onto specific locations such as corners and peaks of base materials to level the thickness of copper deposit. In the presence of a micro profile the diffusion layer tends to be thin at the peaks and thick at the valleys. In this case the micro profile will be exaggerated if it is plated without a leveler. On the other hand, the plating on the peaks will be suppressed and the micro profile will be diminished if a leveler is present. Therefore, the additives play key roles to obtain plating uniformity and physical properties. Many additives were screened during the development of a specific product that can meet the plating performance requirements. Once the additives are selected and optimized, the type of anodes in a plater, VMS, and plating current density need to be optimized as they also have effect on plating performance.

Below is an example on the plating performance from Systek UVF 200 on a board with via size at 60 x 40 µm, finest line width down to 9 µm in a VCP plater. The electrolyte was with a VMS of copper sulfate at 240 g/L, sulfuric acid at 40 g/L, Cl at 50 ppm. The plating current density was at 1.2 ASD, plating duration was 60 minutes, and bath temperature was 25 °C to obtain copper thickness around 12 µm. The plated height variation between fine lines (9 µm wide) and pads (50 µm wide) was 1.7 µm. The cross sections of these features are shown in Figure 1.

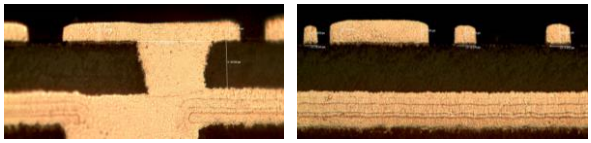


Figure 1. 2-In-1 RDL plating results from Systek UVF 200 electrolyte, CD at 1.2 ASD, 60 min, bath at 25 °C

When the plating current density was increased to 4.5 ASD, plating time was shortened to 15 minutes, bath temperature was at 25 °C, the same plated copper thickness, 12 µm, was obtained. The plated height variations between fine lines and pads were, 2.7 µm, within a die, vias were still filled well without any dimple.

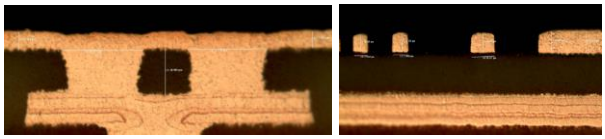


Figure 2. 2-In-1 RDL plating results from Systek UVF 200 electrolyte, CD at 4.5 ASD, 15 min, bath at 25 °C

When the bath temperature was increased to 35 °C, the thickness variation between fine line, 9 µm and pads, 50 µm, dropped to 1.3 µm, excellent uniformity was obtained.

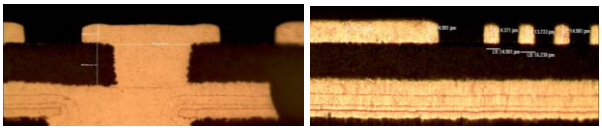


Figure 3. 2-In-1 RDL plating results from Systek UVF 200 electrolyte, CD at 4.5 ASD, 15 min, bath at 35 °C

No voids were observed under such conditions. The evaluation on via formation versus plating time under the current density at 5 ASD indicated that the 60 x 40 µm vias were filled with a bottom-up mechanism. The plated thickness was 15 µm after a plating time of 15 minutes.

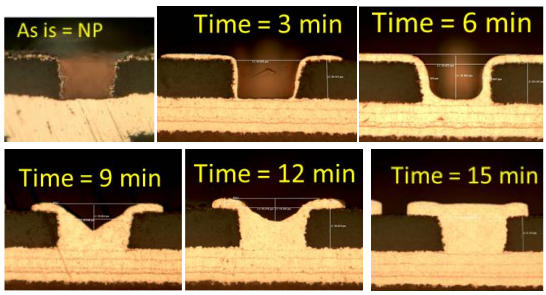
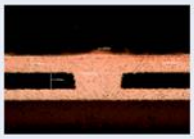
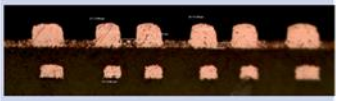
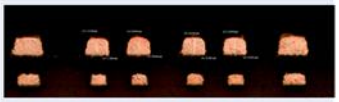


Figure 4. 2-In-1 RDL plating results from Systek UVF 200 electrolyte, CD at 5.0 ASD, bath at 35 °C, plating time was at 3, 6, 9, 12, and 15 minutes.

In the case on the board (from an OEM) with smaller vias, such as the via size at 40x15 µm, finest line down to 14 µm, the via was filled with big bump if the electrolyte with the same VMS as described above, 240 g/L of copper sulfate, 40 g/L of sulfuric acid, 50 ppm of chloride. The electrolyte needs to be adjusted to reduce copper sulfate concentration and increase sulfuric acid concentration to obtain flat via fill, which also improve the plating uniformity within a die when the electrolyte contains 200 g/L of copper sulfate, 100 g/L of sulfuric acid, 50 ppm of chloride.

VMS	Via Dimple (µm)	Via image
240/60/50	-2.15	
200/70/50	-1.2	
200/100/50	0.23	

R value (µm)	Line area image
2.4	
0.88	
0.20	

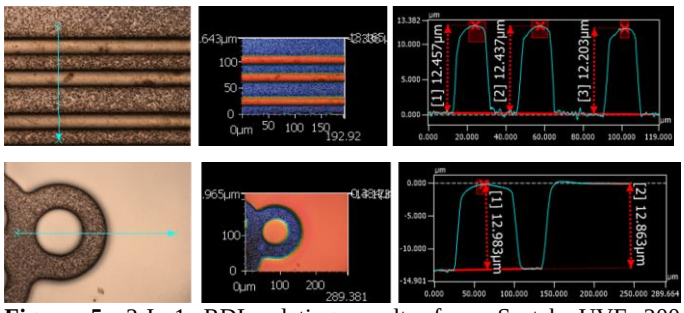


Figure 5. 2-In-1 RDL plating results from Systek UVF 200 electrolyte, VMS concentration was varied.

Features were also evaluated by profilometry, using a Keyence VK-X1000, after dry film was stripped off. Excellent uniformity and flat via fill were observed as shown in Figure 5 when the electrolyte contains 200 g/L of copper sulfate, 100 g/L of sulfuric acid, 50 ppm of chloride.

Panel Uniformity from AMSPT NEXX P500 plater

The ASMPT NEXX P500 plater offers advanced ECD tool features such as single panel process modules, multi-zone anodes, and ion exchange membranes. These features have historically only been available for wafer level ECD tools, but the benefits are becoming compelling in the panel scale as feature sizes shrink to 10 µm line / space and below.

In the panel plating tool, insoluble anodes are used. There are three reasons for this:

1) a solid Cu anode of this size would be extremely unwieldy to install and replace;

2) the segmented anode design described below requires anodes that do not change dimensions over time; and

3) the volume of metal deposited in the plating process is considerably greater than what is seen in wafer tools, and therefore it makes sense to replenish the metal in a more continuous fashion.

Figure 6 shows the contents of one side of a plating cell, including segmented anode and close-edge shield. The panel holder is shown on the left side.

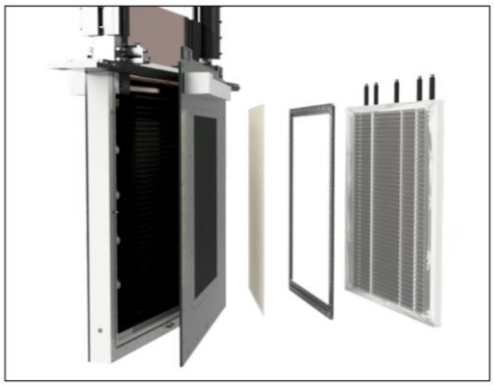


Figure 6. Contents of one side of a plating cell, including segmented anode and close-edge shield. The panel holder is shown on the left side.

The uniformity was measured via profilometry, Keyence VK-X1000, after dryfilm was stripped off, as shown in Figure 7. Five areas were evaluated on RDL fine lines and pad within a die across the board. The measurement on vias were not included in the uniformity calculation to reduce the influence from bump or dimple on a filled via.

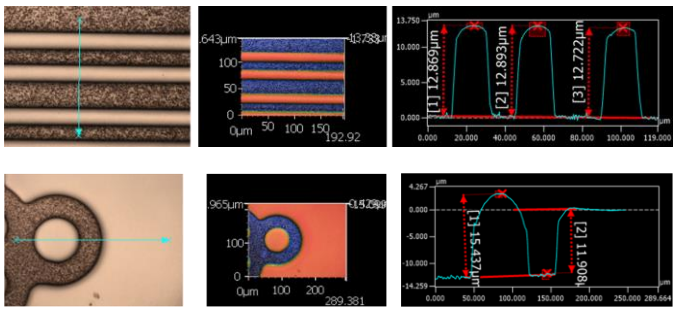
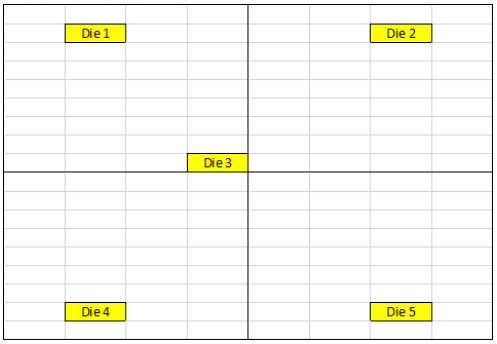


Figure 7. 2-In-1 RDL plating results from Systek UVF 200 electrolyte in AMSPT NEXX P500 plater, CD at 4.5 ASD/35 °C, time was 15 min. Measured by Keyence VK-X1000



Front side	Die 1	Die 2	Die 3	Die 4	Die 5
Fine line 1 height (µm)	12.3	11.4	12.1	12.4	12.1
Fine line 2 height (µm)	11.4	11.4	12.2	12.3	12.0
Fine line 3 height (µm)	12.2	11.6	12.1	12.2	12.1
Pad height (µm)	12.6	11.8	11.7	11.9	11.8
Uniformity WID (µm), H_{max}-H_{min}	1.2	0.4	0.5	0.5	0.3
Uniformity WIP (µm), H_{max}-H_{min}	1.2				

Back side	Die 1	Die 2	Die 3	Die 4	Die 5
Fine line 1 height (µm)	11.7	12.3	12.1	12.1	12.4
Fine line 2 height (µm)	12.0	12.3	12.0	12.4	12.5
Fine line 3 height (µm)	12.0	12.1	11.9	12.3	12.0
Pad height (µm)	12.2	12.3	11.4	11.3	11.7
Uniformity WID (µm), H_{max}-H_{min}	0.5	0.2	0.7	1.1	0.8
Uniformity WIP (µm), H_{max}-H_{min}	1.2				

Table 2. Thickness measurements from a board, 510 mm x 515 mm

The data from measurements showed the plating had excellent uniformity, both within a die and within a panel. The maximum height difference between fine lines and pad within a die (WID) was 1.2 µm, the height variation within fine lines were less than 0.5 µm. The height variation within a panel (WIP) was 1.2 µm on both front and back sides of the board, or around 5% based on the calculation below.

$$\text{Uniformity (WIP\%)} = [(\text{Height}_{max}-\text{Height}_{min})/\text{Height}_{avg}]/2*100$$

Copper Deposit Physical Properties

Physical properties of the plated copper deposit are essential for the reliability of the substrate. A few of the most important physical properties are tensile strength, elongation %, and internal stress. These properties show the tolerance of the deposit to withstand thermal stress and warpage. The additives that include wetter, brightener, and leveler, influence the physical properties of the deposit. Standard testing equipment was used to measure the tensile strength, elongation %, and internal stress. Tensile strength was above 40,000 psi and elongation % was above 18%. Internal stress is an important parameter when plated RDL on thin buildup substrate. With high internal stress, the deposit may warp, and warpage may get worse with time or with temperature. The plated deposits from various current densities all exhibited low stress, below 1.0 Kg/mm^2. The data in Table 3 shows that the physical properties were consistent at various current densities and bath temperatures.

Deposit Copper Grain Structure

FIB-SEM was used to evaluate the copper grain structure under different plating conditions. SEM photos showed the plated copper deposit had equiaxial grain structure, which does not have much variation under different plating current densities.

Plating Condition	**2.0 ASD, 25 C**	**4.5 ASD, 35 C**
Elongation%	22.0%	20.1%
Tensile Strength (PSI)	40.4 K	40.4 K
Internal Stress (tensile)	0.87 (Kg/ mm^2)	0.85 (Kg/ mm^2)

Table 3. Plated copper physical properties.

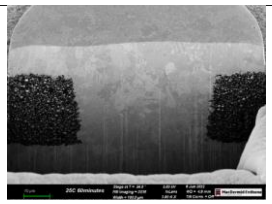
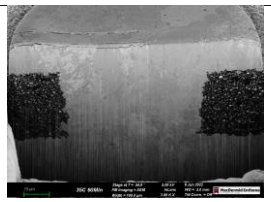
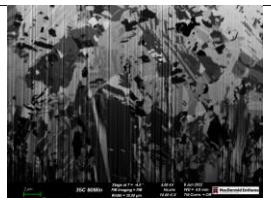
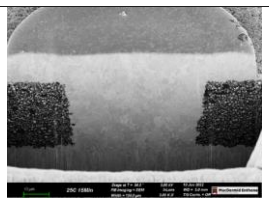
Plating condition	SEM, 3K	Ion-beam image, 10 K
1.2 ASD/60 min/25 C		
1.2 ASD/60 min/35 C		
4.5 ASD/15 min/35 C		

Figure 8. Copper deposit FIB/SEM pictures under different plating current densities.

CONCLUSION

A plating process, Systek UVF 200, was developed for fine line plating and via filling applications, and specifically for IC substrates. The objective of this study was to plate fine lines and vias, while maintaining strict uniformity across the test board. The Systek UVF 200 electrolyte demonstrated this capability in both VCP style tools and a high speed plating tool. The via filling and uniformity across the panel could be adjusted by modifying the VMS, resulting in vias filled without bumps or dimples, and lines/pads with minimum height variation. When the ASMPT NEXX P500 plater was used in the plating process, great uniformity within panel was obtained, 5%, across a 510 mm x 515 mm panel. The physical properties, tensile strength, and elongation passed IPC class III specification. Low internal stress was obtained from the plated samples under different plating conditions. FIB-SEM photos showed the deposited copper had equiaxial grain structure that was consistent when plated at different current densities.

All of the additive components were able to be analyzed with Cyclic Voltammetry Stripping (CVS) analysis.